

MAEDA et al.

Serial No. 10/714,935

Response to Office Action dated July 7, 2006

Please replace the paragraph beginning on page 26, line 18 with the following amended paragraph:

One notable feature of the foregoing circuit block is positioning of the plurality of waveform processing circuits WR (1) through WR (n) which are respectively supplied with output signals of the plurality of flip-flops of the shift register SR. As shown in Figure 1, the waveform processing circuits WR (1) through WR (n) are respectively provided between each adjacent pair pairs of the plurality of flip-flops F/F (1) through F/F (n) which are connected in a form of cascade connection for constituting the shift register SR.

YCC  
7/14/06

Please replace the paragraph beginning on page 34, line 19 with the following amended paragraph:

The first shift register SR1 is constituted of a plurality of flip-flops F/F1(1), F/F1(2), ... F/F1(m), which are supplied with a clock signal SCK1 and a start pulse signal SSP1 as control signals. The second shift register SR2 is constituted of a plurality of flip-flops F/F2(1), F/F2(2), ... F/F2(m), which are supplied with a clock signal SCK2 and a start pulse signal SSP2 as control signals. The first system shift register SR1 and the second system shift register SR2 are adjacently disposed in the vertical direction. In this point, this example is the same as that of Figure 18 having a conventional two-system shift registers sr1 and sr2.